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# 12-Bit, 200 MS/s VXIbus Digital Oscilloscope

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Installation, Operation, Programming, &  
Diagnostic Manual

Model ZT432VXI



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## **HANDLING PRECAUTIONS FOR ELECTRONIC DEVICES SUBJECT TO DAMAGE BY STATIC ELECTRICITY**

The **ZT432VXI** is susceptible to ESD damage. Place instrument or module in a conductive (anti-static) envelope or carrier, when transported. Open only at an ESD approved work surface. An ESD safe work surface is defined as follows:

- 1) The work surface must be conductive and reliably connected to earth ground through a safety resistance of approximately 250 kilohms.
- 2) The surface must NOT be metal. (A resistivity of 30 to 300 kilohms per square inch is suggested.)

Ground the frame of any line-powered equipment, chassis, test instruments, lamps, soldering irons, etc., directly to earth ground. To avoid shorting out the safety resistance, be sure that grounded equipment has rubber feet or other means of insulation from the work surface.

Avoid placing tools or electrical parts on insulators. Do not use any hand tool (such as non-conductive plunger-type solder suckers) that can generate a static charge. Ground yourself reliably, through a resistance, to the work surface using, for example, a conductive strap or cable with a wrist cuff. The cuff must make electrical contact directly with your skin; do NOT wear it over clothing. (Resistance between skin contact and work surface through a commercially available personnel grounding device is typically 250 kilohms to 1 megohm.)

Avoid circumstances that are likely to produce static charges, such as wearing clothes of synthetic material, sitting on a plastic-covered stool (particularly while wearing wool), combing your hair, or making extensive erasures. These circumstances are most significant when the air is dry.

When testing static sensitive devices, be sure DC power is on before, during, and after application of test signals. Be sure all pertinent voltages have been switched off while boards or components are removed or inserted.

### 3.1.1 REVISION HISTORY

Rev	Date	Section	Description
-	9 July 2003		Original Release
1	30 August 2003		Rev_1
2	14 September 2003		Rev_2
3	13 January 2004		Major rewrite of the entire manual

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# 1 Introduction

## 1.1 Description

The ZTEC Instruments model ZT432VXI is the VXIbus version of the ZTEC Instruments 200 million samples per second (MS/s) Digitizer. The ZT432VXI combines a 12 bit, 200 MS/s digitizer with an embedded TMS320VC5409 digital signal processor (DSP) within a single-wide C-sized VXIbus module. Together with the VXIbus host processor and software, the ZT432VXI provides a simple yet powerful way to directly capture and process wide bandwidth video, IF, and low frequency RF signals.

Initiated by trigger events from internal or external sources, the ZT432VXI digitizes a DC to 90MHz signal in user selectable record sizes. The input signal is low-pass filtered to prevent aliasing in the analog-to-digital conversion process. Additional analog signal preprocessing allows selectable coupling, input impedance and input signal range. The digitizer is configured to subdivide the deep, on-board sample memory into segments allowing extremely low re-arm times between consecutive trigger events.

The DSP-based motherboard accommodates very deep synchronous dynamic random-access memory (SDRAM) for storage and post-processing of the numerous sample waveforms. Sample records can be transferred from the SDRAM memory using fast register-based transfers or can be transferred using the SCPI interface to the VXIbus host processor. All digitizer operations are controlled from an intuitive, software based, user interface running on the VXIbus host processor.

## 1.2 Hardware Options

The ZT432VXI is manufactured with different memory options for digitizer fast memory. The digitizer memory size limits the amount of data that can be collected as one waveform or segmented into multiple waveforms with rapid re-arm capability. Note that the installed memory configuration may be identified using the :SYST:MEM? word-serial query.

Memory Option	Total Memory	4 Channel Acquire Memory	2 Channel Acquire Memory
Standard	4 Meg	1 Meg	2 Meg
Option 1	8 Meg	2 Meg	4 Meg

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### 1.3 Contact Information

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To contact ZTEC for technical support please visit our web site and use the tech support form. Our web address is:

**[www.ztec-inc.com](http://www.ztec-inc.com) Web**

We can also be reached by phone at:

**505.342.0132**

## Unit Installation & Configuration

### 2.1 Hardware Installation & Configuration

#### 2.1.1 Hardware Installation

The ZT432VXI may be installed into any C-size VXIbus mainframe, using any slot except slot 0 (zero), which is reserved for the chassis controller. Before installing the ZT432VXI into the mainframe, the ZT432VXI logical address must be assigned (refer to Section 2.1.3). After setting the logical address, slide the ZT432VXI into the VXIbus mainframe until the backplane P1 and P2 connectors are mated properly. Once the module is seated in the mainframe, tighten the two captive screws on the ejector handles to secure the ZT432VXI into the mainframe.

#### 2.1.2 Mainframe Requirements

The ZT432VXI consumes approximately 42.5 W of power distributed among the backplane voltages as described in Appendix A. In order to dissipate this heat, *the VXIbus mainframe must provide at least 11 cubic feet per minute (CFM) of airflow to the slot in which the ZT432VXI is installed.* Failure to meet this requirement may damage the ZT432VXI.

#### 2.1.3 Logical Address Switches

The ZT432VXI logical address is statically configured to any address from 01 to FE (254). Logical address 00 is reserved for the VXIbus resource manager and logical address FF (255) is reserved for VXIbus modules supporting dynamic configuration. The logical address for the ZT432VXI must be assigned by setting the two hexadecimal rotary switches accessible through cut-outs at the rear of the unit. Figure 2-1 shows the switch location on the ZT432VXI module. The most significant digit of the address is at the left when viewed from the rear of the unit with the PCB below the VXIbus connectors.

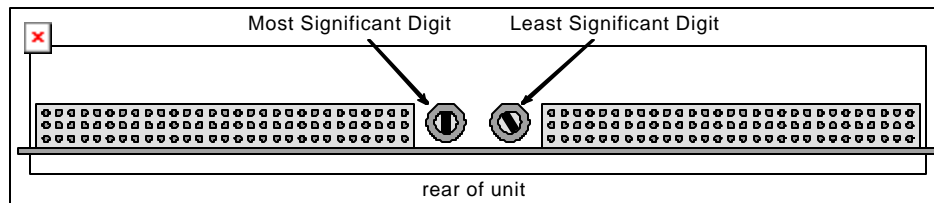


Figure 2-1: Logical Address Switch Location

#### **2.1.4 Backplane IACK\* And BGn\* Jumpers**

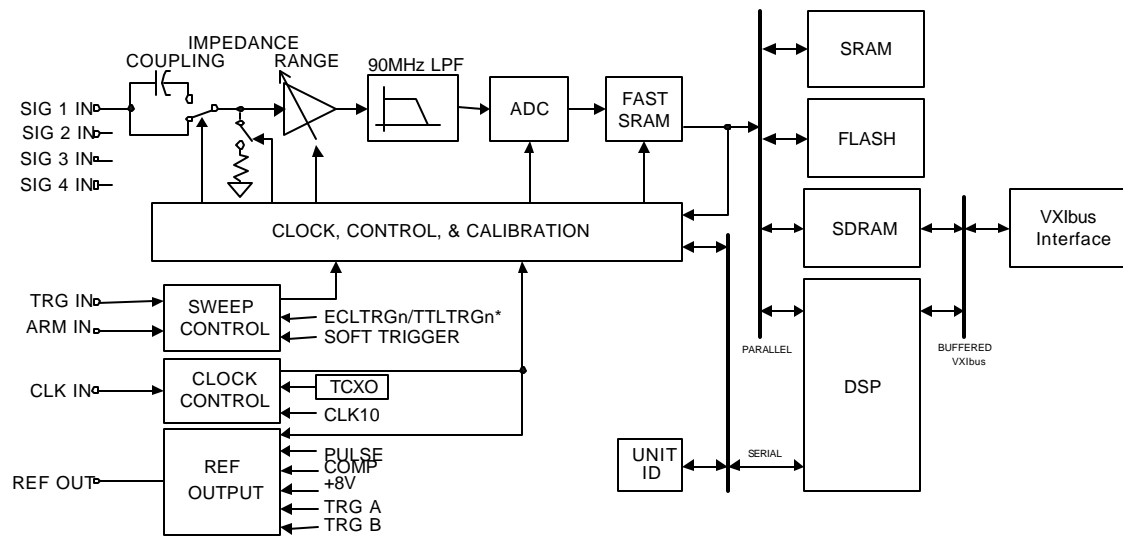
The ZT432VXI is an interrupting device and uses the IACKIN\* and IACKOUT\* backplane signals. The mainframe must be configured to OPEN the connection between these two signals for the slot in which the ZT432VXI is plugged into the P1 connector. If present, ensure that the backplane IACK\* jumper is in the OPEN position according to the manufacturer's guidelines. The ZT432VXI is a slave and does not use the BGnIN\* or BGnOUT\* signals. The ZT432VXI is internally jumpered to transparently pass the BGn\* signals through to the next slot. Consequently, the backplane BGn\* jumpers can be configured in either position and shall not affect the proper operation of the VXIbus system.



## Device Operation

### 3.1 Functional Description

A functional block diagram of the ZT432VXI is shown in Figure 3-1. ZT432VXI functionality is divided into two segments, (1) the 200 MSPS, 12-bit Digitizer Submodule and (2) the VXIbus DSP Baseboard used to provide command and control functions, external interfacing, post-processing, and peripheral clock, trigger and output features.



**Figure 3-1: Functional Block Diagram**

ZT432VXI signal blocks have the following functions

The signal path signal processing is as follows:

- 1) COUPLING – This control is used to select either AC or DC coupling
- 2) IMPEDENCE – This control is used to select either 50 ohm or 1 Meg ohm input impedance
- 3) RANGE – This section is used to scale the input signal to the ADC input range
- 4) 90MHz LPF – The 90 MHz low pass filter limits the input bandwidth to prevent aliasing of high frequency signals into the band of interest
- 5) ADC – 12 bit analog to digital converter
- 6) FAST SRAM – Capture memory for the ADC
- 7) CLOCK, CONTROL, & CALIBRATION – This is the interface logic for the converter path
- 8) SWEEP CONTROL – This is the interface and control of the trigger circuitry. Trigger and arm signals from the instrument front panel, VXI backplane or controller are used to gate the waveform capture

- 9) CLOCK CONTROL – The clock controller selects the clock source for the waveform capture
  - 10) REF OUTPUT – This circuitry is used to select the source for the instruments reference output connector
  - 11) DSP – Digital Signal Processing controller for dealing with waveform math
  - 12) SRAM – Memory used by the DSP controller
  - 13) FLASH – Memory used by the DSP controller
  - 14) SDRAM – Memory used by the DSP controller or for direct memory access to the instrument
  - 15) UNIT ID – EEPROM to store the instrument ID information
- 3) VXIbus INTERFACE – VXI bus controller to take care of bus interface housekeeping

### 3.1.1 Input Signal Conditioning

The ZT432VXI digitizer contains analog signal conditioning to optimize the input signal integrity. The input signal is low-pass filtered to prevent aliasing in the analog-to-digital conversion process. Additional analog signal conditioning allows selectable AC or DC coupling, selectable input impedance and selectable input signal range. The input impedance is programmable to either 50 Ohm or 1M Ohm. The programmable input signal ranges include eight selections for each impedance setting as shown in Table 3-1.

A programmable attenuation factor between 0.9 and 1000.0 allows the user to adjust for probe attenuation or cable losses. A digital smoothing filter can be enabled to apply data post-processing that bandwidth limits the signal to 10% of the sampling frequency.

<b>LO-Z INPUT IMPEDANCE (50 W)</b>	<b>HI-Z INPUT IMPEDANCE (1 M W)</b>
±0.05V	±0.25V
±0.1V	±0.5V
±0.125V	±0.625V
±0.25V	±1.25V
±0.50V	±2.5V
±1.0V	±5.0V
±2.5V	±12.5V
±5.0V	±25.0V

Table 3-1: ZT432VXI Input Signal Ranges

# 3

The ZT432VXI also allows either 2 channel or 4 channel operation, selected using the :SENSe:CHANnel:COUNt command. 2 channel operation doubles both the highest sample rate and waveform record size available with 4 channel. When using 2 channel operation, either channels 1 and 2 or channels 3 and 4 may be selected as the active channels.

The following shows an example command sequence that configures the input signal conditioning of the ZT432VXI.

```
:INP:COUP DC      set coupling to DC
:INP:IMP 1E6      set input impedance to high impedance
:INP:ATT 1.0      set input probe attenuation factor to 1.0
:INP:SMO:STAT ON  set input digital smoothing filter on
:VOLT:RANG:PTP 10 set input range to 10 Vpp
```

## 3.1.2 Horizontal Sweep Controls

The horizontal sweep controls enable the user to adjust the sample rate and timing of the waveform capture process. The sweep controls include including record length, trigger reference point, clock source, and sweep mode.

The record length and corresponding record sweep time are controlled using the sweep commands :SENSe:SWEep:TIME and :SENSe:SWEep:POINt. The record length is programmable between 256 samples and the full digitizer memory length (2 MSamples or 4 MSamples depending upon channel configuration and order option). Note that using the multiple record capture feature, the digitizer memory can be segmented into numerous smaller waveforms for rapid collection of many waveforms. The ZT432VXI provides 19 samples rates as shown in Table 3-2.

The ZT432VXI provides a flexible trigger to record timing adjustment enabling pre-trigger, post-trigger, or delayed trigger storage. Figure 3-2 depicts five sweep reference scenarios. The trigger location within the waveform can be programmed between 0% (start of waveform) and 100% (end of waveform) using the :SENSe:SWEep:OREFERENCE:LOCation command.

SAMPLE RATE	2 CHANNEL MODE	4 CHANNEL MODE
25 kS/s		X
50 kS/s	X	X
100 kS/s	X	X
200 kS/s	X	
250 Ks/S		X
500 kS/s	X	X
1 MS/s	X	X
2 MS/s	X	
2.5 MS/s		X
5 MS/s	X	X
10 MS/s	X	X
20 MS/s	X	
25 MS/s		X
50 MS/s	X	X
100 MS/s	X	X
200 MS/s	X	X (interpolated)
400 MS/s	X (interpolated)	X (interpolated)
1 GS/s	X (interpolated)	X (interpolated)
2 GS/s	X (interpolated)	

**Table 3-2: ZT432VXI Sample Rates**

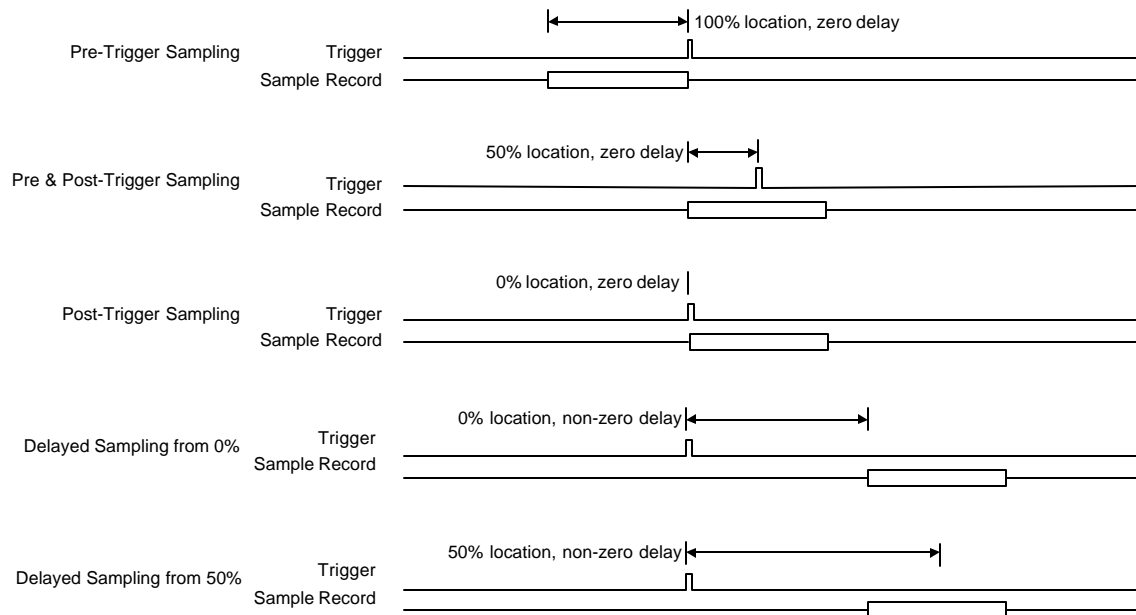
A timing delay between this reference location and the trigger event is also programmable with the `:SENSe:SWEep:OFFSet:TIME` command. This timing delay adjusts the trigger to reference position in either the positive time or negative time direction. Positive values move the end-of-capture further from the trigger event and consequently move the offset reference to the left. Negative values move the end-of-capture closer to the trigger event and consequently move the offset reference to the right. This allows the waveform capture to be delayed long after the trigger event. The negative time offset is limited to the record capture start time which is equivalent to 100% reference location with no time offset.

The maximum cumulative delay between the trigger event and the end of the waveform record is 650 seconds. The cumulative delay is defined as follows:

$$\text{cumulative delay} = ((1 - \text{:SWE:OREF:LOC}) * \text{:SWE:TIME}) + \text{:SWE:OFFS:TIME}$$

Note that a trigger delay of 0.0 seconds causes the trigger position to be set by the offset reference location only, forcing the trigger to lie within the waveform.

# 3



**Figure 3-2: ZT432VXI Trigger to Sample Record Timing Examples**

The ZT432VXI digitizer supports flexible time-base reference and ADC sampling clock input configurations. The source of the time-base reference is selectable between an internal temperature compensated crystal oscillator (TCXO) or the VXIbus backplane CLK10. The internal TCXO reference provides  $\pm 2.5$  ppm frequency accuracy. This 10 MHz time-base is used to generate the sampling clock for the digitizer. The reference oscillator source is selected using the `:SENSe:ROSCillator:SOURce` command.

The ZT432VXI digitizer provides two sweep modes: automatic and normal. Automatic mode forces a trigger event when one is not detected for more than 100 ms. Normal mode will wait indefinitely for a trigger event before capturing data. Sweep mode is configured using the word-serial command `:SWE:MODE`.

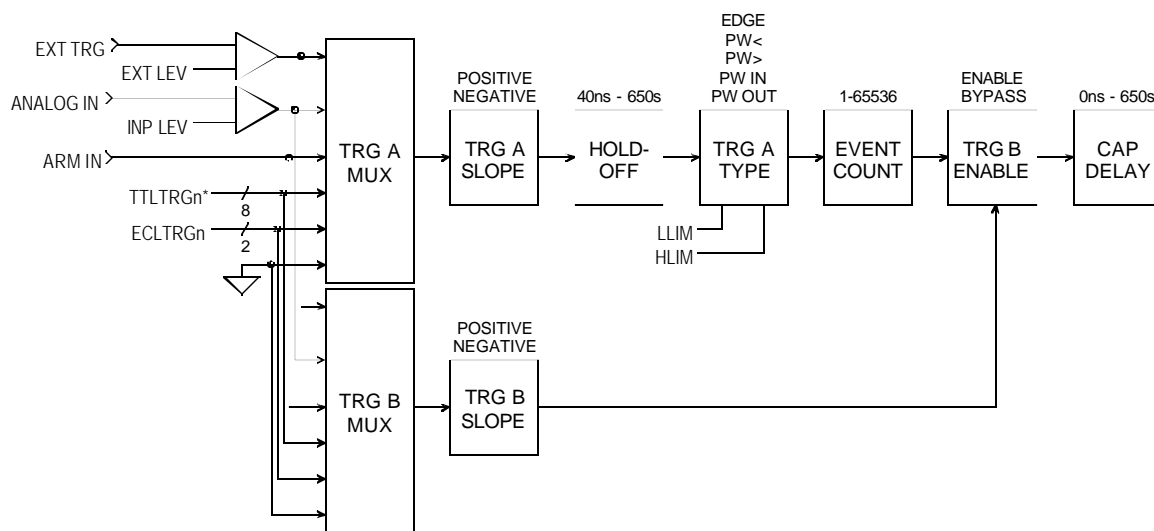
The following shows an example command sequence that configures the sweep controls of the ZT432VXI.

```

:ROSC:SOUR INT    select the internal TCXO reference oscillator
:SWE:POIN 1000    set capture size to 1000 points
:SWE:TIME 10 US   set capture time to 10 usec
:SWE:OREF:LOC 50  set position offset to 50%
:SWE:OFFS:TIME 0  set time offset to 0
:SWE:MODE NORM    turn off auto trigger
  
```

### 3.1.3 Triggering

The ZT432VXI provides very flexible trigger detection circuitry. Figure 3-3 shows a functional block diagram of the trigger detection process. Each of the analog trigger sources (external trigger input and 4 analog signal inputs) have a programmable threshold level to convert from an analog input to a binary trigger state. These five trigger sources, the eight VXIbus backplane TTLTRGn\* triggers, the two VXIbus backplane ECLTRGn triggers, the ARM input signal, or a software-trigger can be selected as the trigger sources for both triggers A and B.



**Figure 3-3: Functional diagram of trigger detection**

Both selected trigger sources can be programmed to trigger on the positive or negative slope. Trigger A is applied to the hold-off circuitry that ignores trigger events for a programmable time window. Trigger A can be selected for edge or pulse width trigger types. Pulse width triggering enables the trigger circuit to detect: pulses shorter than a lower limit time, longer than an upper limit time, within an upper and lower limit time window, or outside an upper and lower limit time window. The resulting trigger events are counted for 1 to 65536 times before latching the primary trigger A event. If enabled, a secondary trigger B source can be used to further qualify trigger detection after the primary trigger A event is latched. When the final trigger event is qualified, the capture delay circuitry creates the acquisition gate timing as defined earlier within the sweep description. The following shows an example command sequence that configures the trigger controls of the ZT432VXI.

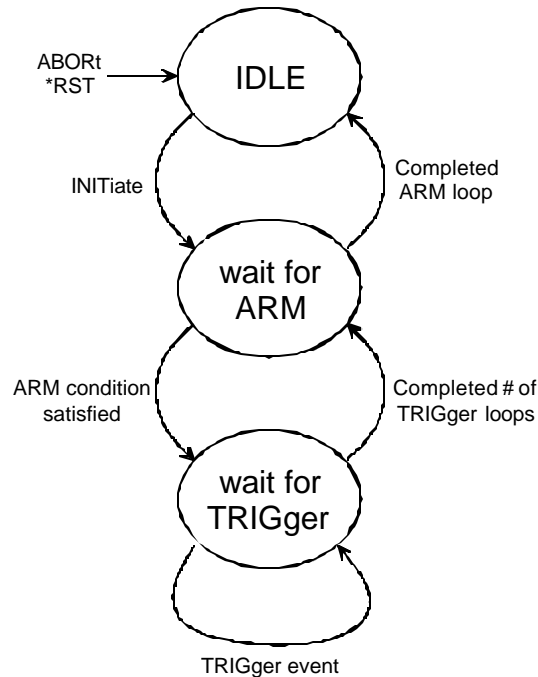
```

:TRIG:TYPE EDGE    set trigger A type to edge
:TRIG:SLOP POS     set trigger A slope to positive
:TRIG:INP1:LEV 0.5 set input trigger level to 0.5 volts
:TRIG:SOUR INP1    set trigger A source to analog input 1
:TRIG:ECO 1        set trigger A event count to 1
:TRIG:HOLD 40e-9   set trigger A holdoff to 40 ns
:TRIG:B:STAT OFF   bypass trigger B

```

### 3.1.4 Waveform Capture Cycle

The ZT432VXI digitizer uses an ARM-TRIGger model to control data acquisition. As shown in Figure 3-4 there are two distinct levels of event detection: ARM detection and TRIGger detection. All acquisition cycles are started with the INITiate command. Upon receiving an INITiate, the ZT432VXI will sequence into the “wait for ARM” state. When the ARM source goes active or if the ARM source is set to immediate, the ZT432VXI will sequence into the “wait for TRIGger” state. When a TRIGger event is detected, the ZT432VXI will capture a waveform. The TRIGger loop will cycle for a selected number of times, saving the waveform associated with each pass. When the requested number of trigger loops have been completed, the ZT432VXI will sequence back to the IDLE state. An ABORt or \*RST command will immediately end the capture sequence and return the instrument to the IDLE state from any other state.



**Figure 3-4: State Diagram for Control Status Register capture cycle bits**

Note that the ZT432VXI digitizer supports memory segmentation that allows multiple waveforms to be captured within a single ARM cycle. The ZT432VXI allows segmented waveform lengths between 256 Samples and 4 MSamples (depending on the number of active channels and order option). Between 1 and 1024 waveforms may be captured within the fast digitizer memory for a single ARM cycle (depending on waveform length). The rapid re-arm capability of the digitizer allows the capture of multiple waveforms occurring in quick succession with less than 40 usec re-arm time.

The following shows an example command sequence that configures and starts a capture cycle on the ZT432VXI.

```
:ABOR abort any on-going operations
:TRIG:COUN 2 set to capture two waveforms in single capture cycle
:ARM:SOUR ARM set arm source to the external ARM input signal
:ARM:SLOP POS set arm slope to positive
:INIT:IMM initiate a capture cycle
*TRG Immediately and bypasses the trigger count (do this if necessary)
```

### 3.1.5 Status Reporting

The ZT432VXI uses the status reporting registers as defined in IEEE Std 488.2-1992. These registers include the:

- Status Byte,
- Operation Status Register,
- Questionable Status Register,
- Questionable Event Enable Register,
- Operation Status Register,
- Operation Event Enable Register,
- Standard Event Register, and
- Standard Event Enable Register.

Figure 3-5 shows the data structures for the status registers on the ZT432VXI. This status structure contains status registers, event registers, and event registers.

Status registers reflect the current status of the ZT432VXI. Status registers change state whenever their corresponding signals change state.

Event registers reflect past events that have occurred on the ZT432VXI. Event registers are set high and latched when an event occurs and are reset only when the VXIbus commander reads that event register or issues a \*CLS command.

Event enable registers provide a means to enable and disable events from propagating to the next level in the data structure tree. Event enable registers are set and cleared by the VXIbus commander.

Figure 3-5 shows the manner in which an event propagates through the event and condition registers on the ZT432VXI. When an event occurs on the ZT432VXI, a cascade of events can propagate through the module and culminate in an interrupt of the VXIbus commander, if the appropriate event enable registers are set.

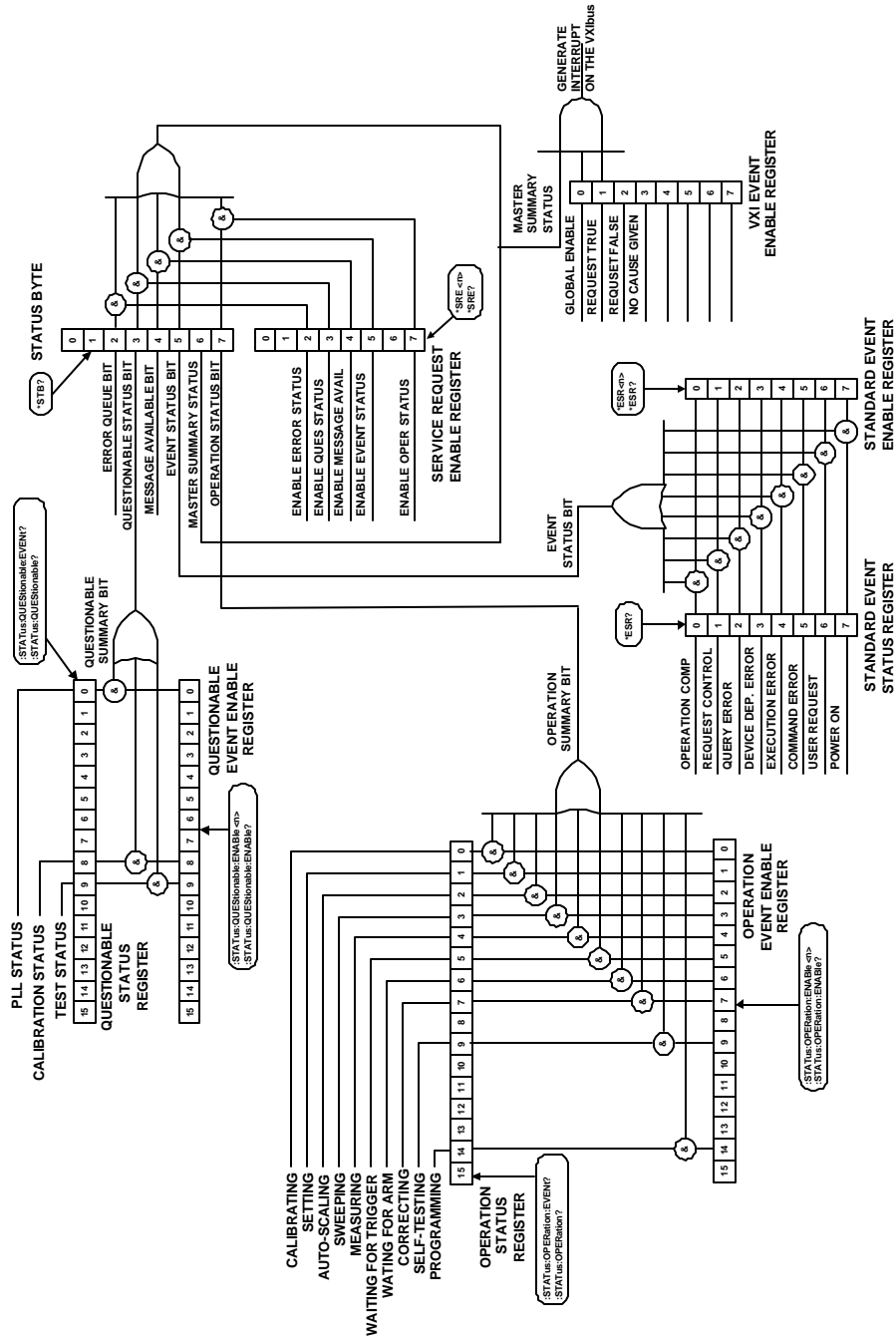


Figure 3-5) Status reporting tree structure

**Figure 3-5: Status reporting tree structure**

### 3.1.6 Waveform Data

Waveform data used by the ZT432VXI is maintained in two structures, a sample record and a preamble. The sample record is an array of 16 bit values containing a 12 bit signed integer value and 4 bits of status or a 16 bit signed integer. The 16 bit format is useful to add precision to waveform math or waveform averaging. The mixed sample/status format is used by the analog input channels and the 16 bit integer format is used by all other sources. The 4 bits of status on the analog input channels may be disabled using the :TRACe:FLAGs:STATe command, leaving additional bits for signal information. The mixed sample/status word is described below:

Bits 15 to 4	msbs	12 bit signed integer waveform sample
Bit 3		digitizer input over-range condition, 1 = over-range
Bit 2		detected trigger event, 1 = trigger detected
Bit 1		raw sampled trigger, 1 = input signal above threshold
Bit 0	lsb	start-of-data marker, 1 = start of data

The preamble provides information necessary to convert the 16 bit integer waveform samples to/from time and voltage values. Preamble information is divided into three blocks, header information, time axis information, and voltage information as described below:

#### Header Information

Sample Data Format	1 = 8 bit ASCII, 2 = 8 bit integer, 3 = 16 integer, 4 = 32-bit integer, and 5 = floating point
Waveform Type	1 = normal voltage-time waveform, 2 = averaged voltage-time waveform, 3 = envelope waveform
Count	the number of waveforms processed to produce an output, = average count for averaged or enveloped waveforms, = the total waveforms captured for a multiple waveform acquisition

#### Time Axis Information

Size	the number of samples in the sample record
Increment	the time interval between samples
Offset	time between the trigger event and the first sample in the sample record
Reference	the record time stamp read from the unit free-running 100 nsec resolution, 1 second rollover timer

#### Voltage Axis Information

Size	the number of waveforms in the sample record, = 2 for enveloped waveforms, = 1 for all others
Increment	the voltage interval between samples
Offset	the voltage offset between 0.0 V and the sample record "0" code
Reference	the waveform number, = the waveform sequence number for a multiple waveform acquisition, = 1 for all others

To recreate a waveform from the preamble and sample record use the following relationships:

Sample Time = time offset + (sample number \* time increment)

Sample Voltage = voltage offset + (sample integer value \* voltage increment)

### 3.1.7 Waveform Download

The ZT432VXI provides two methods for waveform access by the host processor: word-serial access and VXIbus A32 register-based access.

Word serial access enables the host processor with a universally available means to download waveform data one byte at a time over the message-based, word-serial interface using the TRACe:DATA? command. When the word-serial access is being used the command interface shifts into a binary mode to transfer data. Once a transfer has been started the command interface is locked out until the transfer is complete. If necessary use the word-serial CLEAR command to abort the transfer. Word-serial transfers use the low address area of VXIbus A32 memory to build the transfer. Previous contents of this memory are over-written. The transfer format is shown below:

#nccccddd.... Where “#” is the binary download prefix, the ASCII “pound sign”,  
“n” is the number of transfer byte count digits, a decimal number in ASCII.  
“cccc” is the transfer byte count, a decimal number in ASCII,  
“ddd...” are the binary data bytes, and

An example of this format is #42000<bytes>, which will transfer 2000 bytes of data.

The register-based access bypasses the interface overhead of the word-serial protocol and reads/writes waveform samples directly from VXIbus A32 memory, providing significantly faster data transfer speeds. Register based access requires that the chassis controller support A32 access.

When the A32 download mode is set to automatic, digitizer data is automatically copied to VXIbus A32 SDRAM memory upon completion of a capture cycle. The maximum possible number of acquired waveforms in shared VXIbus A32 memory depends upon the digitizer fast memory size and the waveform record length. With the largest factory -installed digitizer memory and the smallest record length, the maximum number of waveforms is 1024.

The ZT432VXI can also be commanded to transfer selected waveforms to the low address area of the unit VXIbus A32 SDRAM memory with the :TRACe:DOWNload command. Each captured analog input waveform is identified by a number ranging between 1 and 1024. The number of acquired waveforms can be determined by issuing the word-serial query :TRIGger:COMplete?. In order to download a waveform from A32 memory, the host VXIbus processor must identify the waveform address and length and then download each waveform.

A timestamp of the waveform trigger time is stored for every captured waveform. The timestamp uses a free-running timer with 100 ns resolution and a 1 second wrap period.

The following shows an example command sequence that enables and downloads captured waveform data.

```
:TRAC:DOWN:STAT ON set automatic waveform download to A32 memory
:TRIG:MODE SINGLE set trigger acquisition mode to single
:TRIG:COUN 2 set to capture two waveforms in single capture cycle
:ARM:SOUR IMM set arm source to immediate
:INIT:IMM initiate a capture cycle
```

wait for capture cycle to complete – force triggers with \*TRG if necessary

```
:TRIG:COMP? Query number of waves captured (2 for this example)
:TRAC:TIM? 1 Query timestamp for waveform 1
:TRAC:ADDR? INP,1 Query address and length in A32 space for waveform 1
```

download waveform 1 from specified address in A32 memory on ZT432VXI

```
:TRAC:TIM? 2 Query timestamp for waveform 2
:TRAC:ADDR? INP,2 Query address and length in A32 space for waveform 2
```

download waveform 2 from specified address in A32 memory on ZT432VXI

### 3.1.8 Reference Waveforms

The ZT432VXI allows the user to save and download up to 4 reference waveforms. The reference waveforms, REF1-4, are stored in non-volatile Flash memory and are maintained when the unit is powered off. These waveforms are limited to record sizes of 32,752 samples or less.

The following shows an example command sequence that saves and accesses a reference waveform on the ZT432VXI.

```
:TRAC:REF1:COPY INP,2 copies the second captured waveform from analog input 1 to
REF1 memory
:TRAC:DATA REF2 copies a waveform from the host to REF2 memory
:TRAC:ADDR? REF1 query address and length in A32 space for REF1
```

### 3.1.9 Instrument States

The ZT432VXI allows the user to save and recall up to 48 instrument configuration states. These states record the input settings, horizontal sweep settings, trigger settings, and capture settings. The current instrument state can be saved and recalled later. All states are stored in non-volatile Flash memory and are maintained when the unit is powered off. The factory reset state can also be restored by command. The IEEE-488 commands \*RST, \*SAV, and \*RCL control the instrument state configuration.

The following shows an example command sequence that saves and recalls an instrument state.

```
*SAV 1      save current instrument state to state 1
*RCL 3      recall previously-saved instrument state 3
```

### 3.1.10 Outputs

The ZT432VXI can drive several signal outputs over the front panel reference output connector and the VXibus backplane TTLTRGn\* and ECLTRGn lines. Each output can be independently configured with unique source and enable controls.

The front-panel REF OUT signal source can be selected from the following sources:

- a precision +8V voltage reference
- a 500 Hz TTL probe compensation output
- the selected 10 MHz reference oscillator
- the Trigger A event
- the Trigger B event
- a 10 ns TTL pulse at 1 ms repetition rate

Positive or negative polarity is selectable for all VXibus backplane outputs. The signal source for the VXibus backplane TTLTRGn\* and ECLTRGn output lines can be selected from the following:

- the selected Arm signal
- the Trigger A event
- the Trigger B event
- the OPC event that occurs when all ZT432VXI operations are complete.

The following shows an example command sequence that sets up the outputs on the ZT432VXI.

```
:OUTP:ECLT0:SOUR ARM set ECLTRG0 source to selected ARM event
:OUTP:ECLT0:POL INV set ECLTRG0 output polarity to inverted
:OUTP:ECLT0:STAT ON enable ECLTRG0 output to VXIbus backplane

:OUTP:TTLT4:SOUR TRGA set TTLTRG4* source to selected TRIGger A event
:OUTP:TTLT4:POL NORM set TTLTRG4* output polarity to non-inverted
:OUTP:TTLT4:STAT ON enable TTLTRG4* output to VXIbus backplane

:OUTP:REF:SOUR COMP set front panel REF OUT source to 500 Hz clock
:OUTP:REF:STAT ON enable front panel REF OUT output
```

### 3.1.11 VXIbus Interface

The VXIbus interface of the ZT432VXI combines an A16 message-based command interface and an A32 register-based memory interface. The interface to the VXIbus host processor is accomplished via the message-based protocol using the Data-Low Register and the Response Register. Programming of this message-based interface is discussed in detail in Sections 4 and 5.

In addition to the message-based interface, waveform data is available within A32 register-based memory. This memory is used to transfer the large blocks of digitized signal data from the ZT432VXI.

Also, the ZT432VXI can interrupt the VXIbus host processor using one of the backplane IREQn\* lines. The interrupt level is assigned by the host processor using low-level VXIbus commands.

In general, all control on the module is accomplished through the VXIbus host processor via the VXIbus backplane. The host processor sends commands and queries to the ZT432VXI to enable its functions and read its status. The command set includes the low-level VXIbus configuration commands, IEEE 488.2 common commands, commands to configure the gain, threshold, and time settings, commands to enable event latching, and a command to enable interrupts. The query set includes low-level VXIbus configuration queries, IEEE 488.2 common queries, queries of the gain, threshold, and time settings, queries of current module conditions, and queries of latched module events.

### 3.1.12 LED Indicators

The ZT432VXI has four front panel LED indicators. These indicators provide visual feedback on different status items of the ZT432VXI during normal operation. Diagnostic codes are displayed during the unit boot process and before the unit is ready for VXIbus operations. If after 5 seconds the LED indicators display a fixed pattern with the RDY LED off, contact ZTEC Instruments for more information. When lit, the unit is either in progress on the current operation or awaiting an input to complete the current operation. The TRG LED provides an indication that a trigger event has occurred to synchronize a waveform acquisition. The TRG LED pulses during each trigger event. To summarize, the LED functions are listed as follows.

# 3

---

RDY	indicates that unit has passed power-up self-diagnostics and is ready for use, flashes when error status is detected
VXI	flashes to indicate that a VXI access has occurred or that the VXIbus MODID line is asserted
BUSY	indicates that the unit is busy, when lit indicates one of the following operations is pending: auto-scale, calibration, self-test, data capture, or data storage
TRG	flashes to indicate that a trigger event was recognized



# 4

## VXI Interface

### 4.1 Interface Description

The ZTEC Instruments model ZT432VXI is a message-based VXIbus module that supports the protocols of a VXIbus Instrument and a VXIbus 488.2 Instrument and is compliant with the instrument specifications outlined in the VXI-1 Revision 1.4 and IEEE Standard 488.2-1992 specifications. In accordance with these specifications, the ZT432VXI supports a number of levels of communication protocols including low-level VXIbus word-serial commands, IEEE 488.2 common commands, and high-level ZT432VXI-specific commands. This section describes the low-level VXIbus interface of the ZT432VXI. Section 5 describes the high-level word-serial commands for the ZT432VXI.

### 4.2 VXIbus Interface

The ZT432VXI is an A16 message-based slave module with A32 register-based memory. As an A16 message-based slave, the ZT432VXI receives commands via the VXIbus word-serial protocol. In order to support the word-serial protocol, the ZT432VXI provides a set of A16 accessible registers as shown in Table 4-1. Each of the registers shown in Table 4-1 is defined by detailed bit descriptions given in Tables 4-3 to 4-11. The ZT432VXI also provides A32 register-based memory that is directly address-mapped in the VXIbus A32 address space. The A32 address space is used to transfer large data blocks to and from the ZT432VXI. Table 4-2 shows the ZT432VXI A32 address map. Both the A16 and A32 interfaces support 16 bit data transfers only.

OFFSET	FUNCTION	TYPE
00 <sub>16</sub>	ID Register	Read-Only
02 <sub>16</sub>	Device Type Register	Read/Write
04 <sub>16</sub>	Status/Control Register	Read/Write
06 <sub>16</sub>	Offset Register	Read/Write
08 <sub>16</sub>	Protocol Register	Read-Only
0A <sub>16</sub>	Response Register	Read-Only
0C <sub>16</sub>	unused	
0E <sub>16</sub>	Data Low Register	Read/Write
10 <sub>16</sub> -3E <sub>16</sub>	unused	

Table 4-1: VXIbus A16 Address Space

OFFSET	FUNCTION	TYPE	SIZE
00000000 <sub>16</sub> -FFFFFFFE <sub>16</sub>	Digitizer Data Memory (SDRAM)	Read/Write	64M-512M

Table 4-2: VXIbus A32 address space

#### 4.2.1 ID Register

The ID Register is a read-only register located at A16 address offset 00<sub>16</sub>. Reading the ID Register returns the ZT432VXI Device Class, Address Space, and Manufacturer's ID. The Device Class for the ZT432VXI is Message (10<sub>2</sub>). The Address Space for the ZT432VXI is A16/A32 (01<sub>2</sub>). The Manufacturer's ID for the ZT432VXI is that of ZTEC Instruments Inc.: 3712 (0E80<sub>16</sub>). Writing to the ID Register has no effect. Table 4-3 defines the function of each bit in the read-only ID Register.

BIT #	FUNCTION	TYPE	VALUE	MEANING
15-14	Device Class	Read	10 <sub>2</sub>	Message-Based
13-12	Address Space	Read	01 <sub>2</sub>	A16/A32 Memory
11-0	Manufacturer's ID	Read	E80 <sub>16</sub>	ZTEC Instruments

Table 4-3: ID Register Bit Descriptions (read-only)

## 4.2.2 Device Type Register

The Device Type Register is a read-only register located at A16 address offset 02<sub>16</sub>. Reading the Device Type Register returns the ZT432VXI Required Memory and Model Code. The Required Memory for the ZT432VXI varies from 64 Mbytes (5<sub>16</sub>) to 512 Mbytes (2<sub>16</sub>) depending on the installed SDRAM size. The Model Code for the ZT432VXI is 432<sub>10</sub> (1B0<sub>16</sub>). Writing to the Device Type Register has no effect. Table 4-4 defines the function of each bit in the read-only Device Type Register.

BIT #	FUNCTION	TYPE	VALUE	MEANING
15-12	Required Memory	Read	5 <sub>16</sub> to 2 <sub>16</sub>	64 Mbytes to 512 Mbytes
11-0	Model Code	Read	1B0 <sub>16</sub>	ZT432VXI

Table 4-4: Device Type Register Bit Descriptions (read-only)

## 4.2.3 Status/Control Register

The Status/Control Register is a read/write register located at A16 address offset 04<sub>16</sub>. Writing to the Status/Control Register changes the Control Register. Table 4-5 defines the function of each bit in the Control Register. Reading the Status/Control Register returns the contents of the Status Register. Table 4-6 defines the function of each bit in the read-only Status Register.

BIT #	NAME	FUNCTION	TYPE
15	A32 Enable	0: Disable A32 Memory 1: Enable A32 Memory	Write
14-2	unused		
1	SFIInh	0: Enable Sysfail* Driver 1: Inhibit Sysfail* Driver	Write
0	SReset	0: Enable Unit 1: Soft Reset Unit	Write

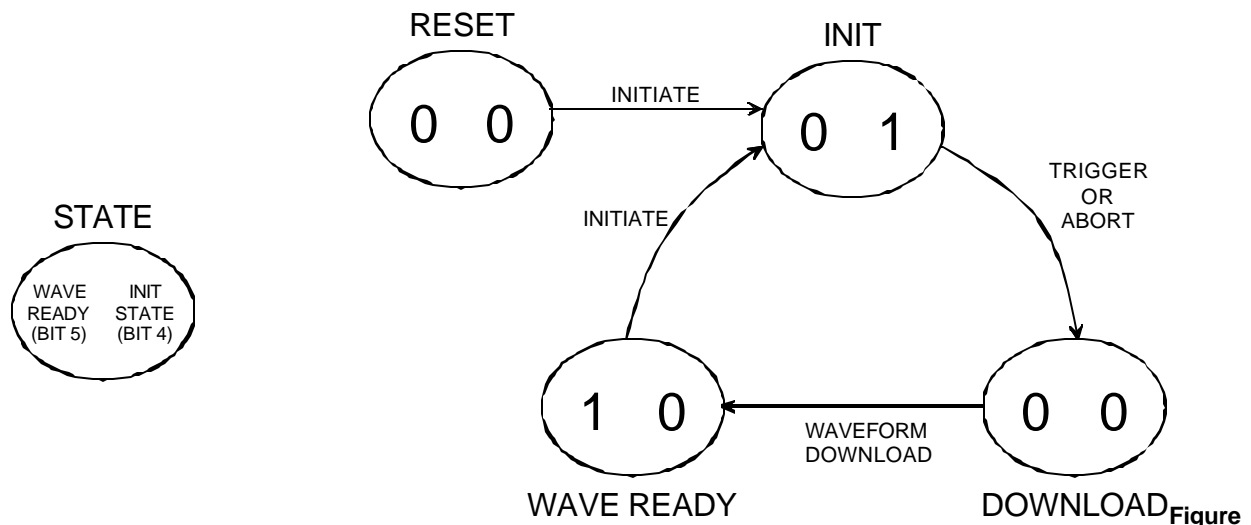
Table 4-5: Control Register Bit Descriptions (write-only)

# 4

BIT #	NAME	FUNCTION	TYPE
15	A32 Active	0: A32 Memory Inactive 1: A32 Memory Active	Read
14	Mod ID*	0: Mod ID Line Driven 1: Mod ID Line Not Driven	Read
13-6	unused	0	
5	Wave Ready	0: Waveforms Not Yet Available 1: Waveform in A32 Memory	Read
4	Initiated	0: Unit In Disarmed State 1: Unit In Initiated State	Read
3	Ready	0: Unit In Configure State 1: Unit In Normal Operation State	Read
2	Passed	0: Unit Failed Self-Test 1: Unit Passed Self-Test	Read
1	SFIInh	0: Sysfail* Driver Enabled 1: Sysfail* Driver Inhibited	Read
0	SReset	0: Unit Enabled 1: Unit Software Reset	Read

**Table 4-6: Status Register Bit Descriptions (read-only)**

Bits 4 and 5 of the Status Register provide the register-based method to poll the current capture state of the ZT432VXI. Figure 4-1 shows the state diagram that relates the condition of these bits to a state in the data capture cycle.



**4-1: State Diagram for Control Status Register capture cycle bits**

#### 4.2.4 Offset Register

The Offset Register is read/write register located at A16 address offset 06<sub>16</sub>. Writing or reading the Offset Register changes or returns the contents of the Offset Register. The Offset Register defines the base address for the ZT432VXI's A32 register-based memory. Only the N most-significant bits of the Offset Register are used, where N varies from 2 to 5 depending upon the installed A32 memory options. Bit 15 is the most-significant A32 address select bit, corresponding to A31 of the address selection. Table 4-7 defines the function of each bit in the Offset Register. Note that this register is configured by the VXIbus Resource Manager, changing this register could result in system failures.

BIT #	NAME	FUNCTION	TYPE
(N) MSBs	A32 Offset	A32 Address Select for VXIbus A31-A(31-N)	read/write
(16-N) LSBs	unused		

Table 4-7: Offset Register Bit Descriptions (read/write)

#### 4.2.5 Protocol Register

The Protocol Register is read-only register located at A16 address offset 08<sub>16</sub>. Reading the Protocol Register indicates the additional communication protocols that are supported by the ZT432VXI. The ZT432VXI supports interrupter capability only. Writing to the Protocol Register has no effect. Table 4-8 defines the function of each bit in the Protocol Register.

BIT #	NAME	FUNCTION	TYPE
15	CMDR*	1: ZT432VXI Has Servant-Only Capability	read-only
14	Signal Register*	1: ZT432VXI Does Not Have A Signal Register	read-only
13	Master*	1: ZT432VXI Does Not Have Master Capability	read-only
12	Interrupter	1: ZT432VXI Has Interrupter Capability	read-only
11	FHS*	1: ZT432VXI Does Not Support Fast Handshake	read-only
10	Shared Memory*	1: ZT432VXI Does Not Support Shared Memory	read-only
9-0	unused	1: unused	read-only

Table 4-8: Protocol Register Bit Descriptions (read-only)

# 4

## 4.2.6 Response Register

The Response Register is read-only register located at A16 address offset 0A<sub>16</sub>. Reading the Response Register returns the status of the communication registers on the ZT432VXI. Writing to the Response Register has no effect. Table 4-9 defines the read-only functions for each bit in the Response Register.

<b>BIT #</b>	<b>NAME</b>	<b>FUNCTION</b>	<b>TYPE</b>
15	Unused	0: unused	read-only
14	Unused	1: unused	read-only
13	DOR	1: Data Out Ready for Byte Request	read-only
12	DIR	1: Data In Ready for Byte Available	read-only
11	ERR*	0: Error in Word Serial Protocol	read-only
10	Read Ready	1: Ready for VXI Read Operation	read-only
9	Write Ready	1: Ready for VXI Write Operation	read-only
8-0	Unused	1: unused	read-only

Table 4-9: Response Register Bit Descriptions (read-only)

## 4.2.7 Data Low Register

The Data Low Register is read/write register located at A16 address offset 0E<sub>16</sub>. Writing or reading the Data Low Register provides the mechanism to transmit word-serial commands between the VXIbus host processor and the ZT432VXI. Writing to the Data Low register causes the ZT432VXI to perform some action. Responses to these actions can be read back from the Data Low Register. Note that the use of this register is strictly defined by the word-serial protocol, writing to this register without following the word-serial protocol requirements could cause interface errors.

<b>BIT #</b>	<b>NAME</b>	<b>FUNCTION</b>	<b>TYPE</b>
15-0	DATA LOW	Word Serial Message To/From ZT432VXI	read-write

Table 4-1: Data Low Register Bit Descriptions (read-write)

### 4.2.8 A32 Address Space

The ZT432VXI contains up to 512 Mbytes (256 MSamples) of register-based memory in the VXIbus A32 address space. This memory is used to store and transfer blocks of acquired data to the VXIbus host processor. In order to maximize data transfer rates, the acquired data is available through direct register-based data transfers. Each digitizer data sample requires two bytes to store the 12-bit data. The SDRAM memory is available as VXIbus A32 address space.

The digitizer data is automatically copied to VXIbus A32 SDRAM memory upon completion of a capture cycle when the A32 download mode is set to automatic (:TRAC:DOWN:STAT AUTO). Otherwise, the ZT432VXI can be commanded to transfer the digitizer data to A32 SDRAM memory (:TRAC:DOWN). The maximum possible number of acquired waveforms in shared VXIbus A32 memory depends upon the digitizer fast memory size and the waveform record length. With the largest factory-installed digitizer memory and the smallest record length, the maximum number of waveforms is 1024. Each waveform in memory is identified by a number ranging between 1 and 1024. The number of acquired waveforms can be determined by issuing a waveform word-serial command (:TRIG:COMP?). In order to download each waveform, the host VXIbus processor must: identify the waveform address and length, and then download each waveform. This procedure is detailed as follows:

- 1) **Identify Waveform Address and Length:** The VXIbus host processor may query the waveform starting address and length of a selected waveform with the word-serial command (:TRAC:ADDR? <src>,<num>). The ZT432VXI responds to this query with the byte address and byte length within the shared VXIbus A32 memory of the selected waveform, where <src> corresponds to the waveform source and <num> corresponds to the waveform number.
- 2) **Download Waveform:** Using the specified address and length, the VXIbus host processor should download each waveform. The VXIbus host processor should repeat this process until all waveforms have been downloaded from the shared VXIbus A32 memory.

Each waveform stored in shared VXIbus A32 memory includes a record preamble that is stored in memory just prior to the actual waveform data. This preamble is twenty 16-bit words in length and can be read at the address location 40 bytes before the address returned by the WAV:ADDR? command. The preamble will allow the user to recover the battery-backed waveform data parameters after a power-off condition (with the battery-backup option). The preamble data is stored in memory as shown in Table 4-11.

FIELD NAME	FORMAT	DESCRIPTION
ID	u16	record ID: $C_{16}NNN_{16}$ where $C_{16}$ is the channel number (0,2,4,6 for channels 1,2,3,4) and $NNN_{16}$ is the record number of multiple trigger capture
FORMAT	u8	data format: 1 = ASCII, 2 = 8-Bit, 3 = 16-Bit, 4 = 32-Bit, 5 = Float
TYPE	u8	data type: 1 = Normal Waveform, 2 = Average, 3 = Envelope
COUNT	u32	record count: number of captured waveforms for multiple trigger capture, or number of waveforms within average or within envelope
XSIZE	u32	horizontal waveform size in points (record size)
XINC	float32	horizontal increment in seconds (sample interval)
XORIGIN	float32	horizontal origin in seconds (trigger location within waveform)
XREF	float32	horizontal reference in seconds (trigger timestamp)
YSIZE	u32	vertical waveform size in number of records (1 for Normal or Average waveform, 2 for Envelope waveform which is represented by high and low records)
YINC	float32	vertical increment in volts (volts per LSB as defined by FORMAT field)
YORIGIN	float32	vertical origin in volts (offset voltage)
YREF	u32	vertical reference in records (record number for multiple trigger capture)

Table 4-11: Preamble Memory Store Format

### 4.3 Low-Level VXIbus Commands

The ZT432VXI is a message-based VXIbus instrument supporting the following low-level VXIbus commands. These commands are sent to the ZT432VXI by reads of and writes to its Data Low register using the VXIbus word-serial protocol. Each command is defined with a unique 16-bit value that is written to the Data Low register. These low-level commands are used by the VXIbus processor at its lowest level of data transfer protocol (transparent to most users). Most users need not concern themselves with these commands, which are listed here in bold type. More information on the low-level VXIbus commands and the word-serial protocol can be found in the VXI-1 Rev. 1.4 VXIbus specification.

#### **BYTE AVAILABLE**

Sends a byte of data to the ZT432VXI.

#### **BYTE REQUEST**

Requests a byte of data from the ZT432VXI.

#### **ABORT NORMAL OPERATION**

Causes ZT432VXI to cease all operations immediately and enter its configuration state.

#### **BEGIN NORMAL OPERATION**

Notifies ZT432VXI that it can begin normal operations and enter its normal-operation state.

**END NORMAL OPERATION**

Causes ZT432VXI to cease all operations in an orderly fashion and enter its configuration state.

**CLEAR**

Clears the VXIbus interface and any pending operations on the ZT432VXI.

**ASYNCHRONOUS MODE CONTROL**

Directs the path of events and responses on the ZT432VXI.

**CONTROL EVENT**

Selectively enables the generation of events by the ZT432VXI.

**READ STB**

Requests the reporting of the Status Byte from the ZT432VXI.

**READ PROTOCOL**

Requests the reporting of protocols supported by the ZT432VXI (EG, I, I4).

**READ PROTOCOL ERROR**

Requests the reporting of the current error state of the ZT432VXI and resets all asserted errors.

**ASSIGN INTERRUPTER LINE**

Assigns a particular backplane IRQn\* line to the ZT432VXI for asserting interrupts.

**READ INTERRUPTER LINE**

Requests the reporting of the current IRQn\* line assigned to the ZT432VXI.

**READ INTERRUPTERS**

Requests the reporting of the number of interrupters within the ZT432VXI (one)

# A

## A. Specifications

### Input Channel Specifications

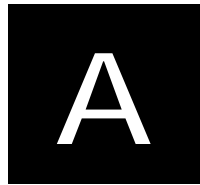
Channels	2 @ Full Sample Rate 4 @ Half Sample Rate
Bandwidth (3dB)	DC to 90 MHz
Full Scale Input Range	100 mVpp to 10 Vpp in 8 steps, 50 $\Omega$ 500 mVpp to 50 Vpp in 8 steps, 1 M $\Omega$
DC offset accuracy	50 $\Omega$ $\pm(1\text{mV} + 0.25\%)$ 1M $\Omega$ $\pm(5\text{mV} + 0.25\%)$
DC gain accuracy	50 $\Omega$ $\pm(1\text{mV} + 0.25\%)$ 1M $\Omega$ $\pm(5\text{mV} + 0.5\%)$
Impedance	software selectable to 1 M $\Omega$    12 pF or 50 $\Omega$
Input VSWR (50 $\Omega$ )	< 1.3:1 DC to 100 MHz < 1.5:1 100 MHz to 250 MHz
Connectors	BNC Female
Coupling	DC or AC AC Coupling Bandwidth: >1 MHz, 50 $\Omega$ AC Coupling Bandwidth: >50 Hz, 1 M $\Omega$

### Digitizer Specifications

Sample Rate interpolation	50 kS/s to 200 MS/s (2 channels), up to 2 GS/s with 25 kS/s to 100 MS/s (4 channels) , up to 1 GS/s with
interpolation	
Resolution	12 bit resolution
RMS Noise	$\leq (100\mu\text{V} + 0.1\% \text{ range})$
Number of Records	1 to 1024, depending on record size
Record Size	256 samples to 2 MSamples 256 samples to 4 MSamples (Option 1)

### Signal Processing Specifications

Reference Waveforms	REF1-4 saved in non-volatile memory (up to 32,752 Samples) REF5-6 saved in volatile SDRAM memory (up to 4 MSamples)
Measurement	Min, Max, Low, High, Average, Amplitude, Peak-to-Peak, Rise Time, Fall Time, Overshoot, Preshoot, +Width, -Width,

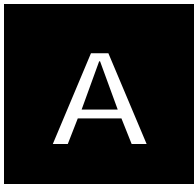


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Period, N <sup>th</sup> Edge Minimum Measurements	Frequency, +Duty, –Duty, Delay, DC RMS, AC RMS, Crossing Time, Time at Maximum Voltage, Time at Voltage, Time at Voltage, Voltage at Time, Cursor
Waveform Math Differentiate	CALC1-2: Add, Subtract, Multiply, Invert, Integrate,
Digital Smoothing Filter	Input Smoothing Filter @ 10% of Sample Rate

### Trigger Specifications

Arm Sources	external arm input      immediate (bypass)      software VXI TTLTRG(0-7)      VXI ECLTRG(1-0)
Trigger Sources input	external trigger input      channels 1 to 4      external arm VXI TTLTRG(0-7)      VXI ECLTRG(1-0)      pattern software
Trigger Level Range	± full scale, channel 1-4 input ±1V, external trigger input
External Trigger Input	±5V maximum, 50Ω input impedance, BNC connector
Analog Trigger Sources	trigger signal for analog channel sources are taken after the associated channel input signal conditioning, including: input coupling, gain, impedance, and bandlimiting
Trigger Detect Modes	edge pulse width < limit pulse width > limit pulse in window pulse not in window
Pulse Width Detect	minimum setting      larger of 1 sample or 5 nano seconds maximum setting      327 microseconds
Trigger Polarity	rising or falling
Trigger Event Counting	multiple trigger event detection: 1-65536 events
Trigger B Functionality	second trigger event source
Trigger Delay	0 ns to 656 seconds
Detection Delay	< 20 nanoseconds
Trigger Holdoff	0 to 656 microseconds
Auto-Triggering Mode	normal or auto trigger
Capture Modes	single      stop after 1 waveforms multiple      stop after N waveforms



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Trigger Event Time Stamp	100 ns resolution, 1 second rollover
Multiple Capture Mode	1 to 1024 records, depending on record size re-arm time approximately 35 microseconds trig accuracy $\pm 5\%$ + offset accuracy

### Front Panel

REFERENCE OUTPUT	BNC
ARM INPUT	BNC
CLOCK INPUT	BNC
EXTERNAL TRIGGER INPUT	BNC
CHANNEL 1-4	BNC

### LED Status Indicators

RDY	indicates that unit has passed power-up self-diagnostics and is ready for use, indicator flashes when error status is pending
VXI	indicates that a VXI access is occurring or that the VXIbus MODID line is asserted
BUSY	indicates that the unit is busy with one of the following operations: auto-scale, calibration, self-test, data capture, or data storage
TRG	indicates that a trigger event was recognized

### Reference Output

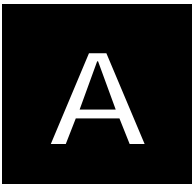
Modes	reference voltage, ground, 10 MHz reference clock, 500 Hz
probe	compensation, or 10 ns pulse @ 1ms rate
Reference Voltage	+8 V $\pm 1\%$ into 10 k $\Omega$ load
Ref Clock, Comp, Pulse	TTL output level

### Arm Input

Level	TTL compatible, 0 to 5 V maximum
Termination	1 k $\Omega$ pullup to +5 V
Logic detection	logic 1 = hold off trigger detection, logic 0 = enable trigger

### External Trigger Input

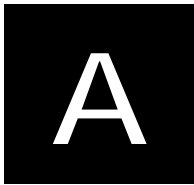
Level	$\pm 1$ V trigger level, $\pm 5$ V maximum range
Coupling	DC coupled



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Impedance

50  $\Omega$



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## External Sampling Clock Input

Level	Square or Sine, 500 mV <sub>pp</sub> to 1 V <sub>pp</sub>
Frequency	1 MHz to 200 MHz 1X sample rate (2 channels) 2X sample rate (4 channels)
Coupling	AC coupled
Impedance	50 Ω

## VXI Interface

Backplane Connection	standard P1 and P2 interface
Command Interface	A16 message based, SCPI compatible
Interrupt Operation	programmable interrupter, level 1 to 7
VXI Trigger Sourcing arm pending complete)	ECLTRG(1-0) and TTLTRG(7-0) may be sourced from signal, main trigger occurred signal, OPC (op signal, positive or negative polarity
Data Interface based	128 Mbytes of VXI accessible DRAM in A32 register-address space

## Other Specifications

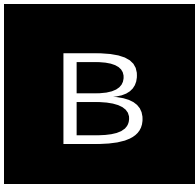
Timebase TCXO or	software selectable 10 MHz timebase, internal 2.5 ppm VXI CLK10
Configuration Save memory	48 instrument configurations, saved in non-volatile memory
Power Consumption	+24 V      0.0 A +12 V      0.1 A,      0.1 A dynamic +5 V      7.0 A,      0.5 A dynamic -24 V      0.0 A -12 V      0.1 A,      0.1 A dynamic -5.2 V      0.7 A,      0.1 A dynamic -2 V      0.1 A,      0.1 A dynamic 42.5 W typical total power

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## B. Errors and Status

### Command Errors

-100	Command error
-101	Invalid character
-102	Syntax error
-103	Invalid separator
-104	Data type error
-105	Get not allowed
-106	Invalid program data separator
-108	Parameter not allowed
-109	Missing parameter
-110	Command header error
-111	Header separator error
-112	Mnemonic too long
-113	Undefined header
-114	Header suffix out-of-range
-118	Query not allowed
-120	Numeric data error
-121	Invalid char in number
-123	Exponent too large
-124	Too many digits
-128	Numeric data not allowed
-130	Suffix error
-131	Invalid suffix
-134	Suffix too long
-138	Suffix not allowed
-140	Character data error
-141	Invalid character data
-144	Character data too long
-148	Character data not allowed
-150	String data error
-151	Invalid string data
-158	String data not allowed
-160	Block data error
-161	Invalid block data
-168	Block data not allowed
-170	Expression error
-171	Invalid expression



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-178 Expression data not allowed

## Execution Errors

- 200 Execution error
- 203 Command protected
- 211 Not ready for trigger
- 212 Not ready for arm
- 213 Already initiated
- 214 Not ready for trigger
- 215 Not ready for arm
  
- 220 Parameter error
- 221 Settings conflict
- 222 Data out of range
- 223 Too much data
- 224 Illegal parameter value
  
- 230 Data corrupt or stale
- 231 Questionable data
- 232 Data has invalid format
- 233 Incompatible version
  
- 240 Hardware error
- 241 Hardware missing
  
- 250 Mass storage error
- 251 Missing mass storage
- 252 Missing media
- 253 Corrupt media
- 254 Media full
- 255 Directory full
- 256 File name not found
- 257 File name error
- 258 Media protected
  
- 260 Expression execution failed
- 261 Math expression execution failed

# B

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## Device Dependent Errors

- 300 Device specific error
- 310 System error
- 311 Memory error
- 313 Calibration memory corrupted
- 314 Configuration memory corrupted
- 315 Manufacturing info corrupted
- 316 Unexpected code reboot
- 317 Table corrupted
- 318 Invalid operational state
- 319 Sample clock PLL unlocked
- 320 EEPROM write failure
- 321 Flash erase failure
- 322 Flash program failure
- 323 Flash verify failure
- 325 SRAM test failure
- 326 DRAM test failure
  
- 330 Self test failed
- 340 Calibration failed
- 350 Queue overflow
  
- 360 Device specific errors
- 361 Input protection activated
- 363 Invalid parameter
- 364 Phase-locked loop unlocked

## Self-Calibration Result Codes

- 0 Calibration successful

## Self-Test Result Codes

- 0 Self-test successful